# CD4067B, CD4097B Types

## CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer

CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

■ CD4067B and CD4097B CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A,B,C,D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067B and CD4097B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (P and PWR suffixes).

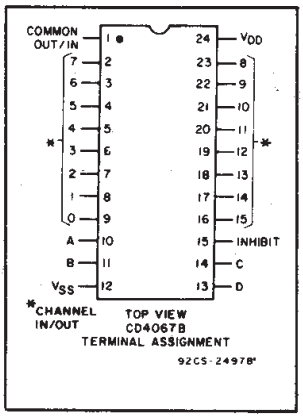
*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

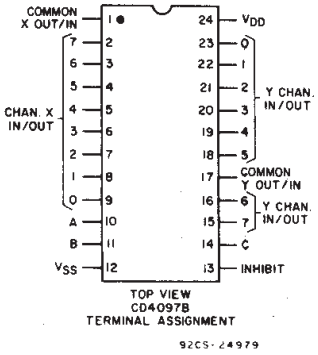
*Features:*

- Low ON resistance: 125 Ω (typ.) over 15 $V_{p-p}$ signal-input range for $V_{DD}-V_{SS}=15$ V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}=10$ V
- Matched switch characteristics: $R_{ON}=5$ Ω (typ.) for $V_{DD}-V_{SS}=15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}=10$ V
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative **Standard No. 13B,** "Standard Specifications for Description of 'B' Series CMOS Devices"

*Applications:*

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating



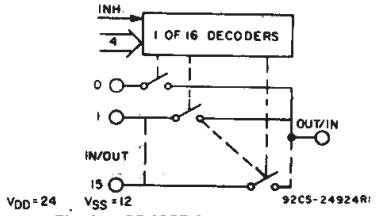




*Fig. 1 – CD4067 functional diagram.*

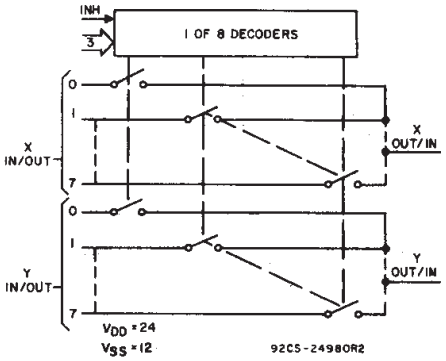



*Fig. 2–CD4097 functional diagram.*

**Recommended Operating Conditions at $T_A = 25°C$ (Unless Otherwise Specified)**

*For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.*

| Characteristic | Min. | Max. | Units |
|---|---|---|---|
| Supply-Voltage Range ($T_A$=Full Package-Temp. Range) | 3 | 18 | V |
| Multiplexer Switch Input Current Capability | – | 25 | mA |
| Output Load Resistance | 100 | – | Ω |

**NOTE:**
In certain applications, the external load-resistor current may include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from $R_{ON}$ values shown in ELECTRICAL CHARACTERISTICS CHART). No $V_{DD}$ current will flow through $R_L$ if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

**CD4067 TRUTH TABLE**

| A | B | C | D | Inh | Selected Channel |
|---|---|---|---|---|---|
| X | X | X | X | 1 | None |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 2 |
| 1 | 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 0 | 7 |
| 0 | 0 | 0 | 1 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 9 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 1 | 1 | 0 | 1 | 0 | 11 |
| 0 | 0 | 1 | 1 | 0 | 12 |
| 1 | 0 | 1 | 1 | 0 | 13 |
| 0 | 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 0 | 15 |

**CD4097 TRUTH TABLE**

| A | B | C | Inh | Selected Channel |
|---|---|---|---|---|
| X | X | X | 1 | None |
| 0 | 0 | 0 | 0 | 0X, 0Y |
| 1 | 0 | 0 | 0 | 1X, 1Y |
| 0 | 1 | 0 | 0 | 2X, 2Y |
| 1 | 1 | 0 | 0 | 3X, 3Y |
| 0 | 0 | 1 | 0 | 4X, 4Y |
| 1 | 0 | 1 | 0 | 5X, 5Y |
| 0 | 1 | 1 | 0 | 6X, 6Y |
| 1 | 1 | 1 | 0 | 7X, 7Y |

## ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{is}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | |
| **SIGNAL INPUTS ($V_{is}$) AND OUTPUTS ($V_{OS}$)** | | | | | | | | | | | |
| Quiescent Device Current, $I_{DD}$ Max. | | | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | | | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | | | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | | | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| ON-state Resistance $V_{SS} \leqslant V_{is} \leqslant V_{DD}$ $r_{on}$ Max. | | 0 | 5 | 800 | 850 | 1200 | 1300 | – | 470 | 1050 | Ω |
| | | 0 | 10 | 310 | 330 | 520 | 550 | – | 180 | 400 | |
| | | 0 | 15 | 200 | 210 | 300 | 320 | – | 125 | 240 | |
| Change in on-state Resistance (Between Any Two Channels) $\Delta r_{on}$ | | 0 | 5 | – | – | – | – | – | 15 | – | Ω |
| | | 0 | 10 | – | – | – | – | – | 10 | – | |
| | | 0 | 15 | – | – | – | – | – | 5 | – | |
| OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max. | | 0 | 18 | ±100* | | ±1000* | | – | ±0.1 | ±100* | nA |
| Capacitance: Input, $C_{is}$ | | −5 | 5 | – | – | – | – | – | 5 | – | pF |
| Output, $C_{os}$ CD4067 | | | | – | – | – | – | – | 55 | – | |
| CD4097 | | | | – | – | – | – | – | 35 | | |
| Feedthrough, $C_{ios}$ | | | | – | – | – | – | – | 0.2 | | |
| Propagation Delay Time (Signal Input to Output | $V_{DD}$ | $R_L$ = 200 KΩ $C_L$=50 pF $t_r, t_f$=20 ns | 5 | – | – | – | – | – | 30 | 60 | ns |
| | | | 10 | – | – | – | – | – | 15 | 30 | |
| | | | 15 | – | – | – | – | – | 10 | 20 | |
| **CONTROL (ADDRESS or INHIBIT) $V_C$** | | | | | | | | | | | |
| Input Low Voltage, $V_{IL}$ Max. | =$V_{DD}$ thru 1 KΩ | $R_L$=1 KΩ to $V_{SS}$ $I_{IS}$<2 μA on all OFF Channels | 5 | 1.5 | | | | – | – | 1.5 | V |
| | | | 10 | 3 | | | | – | – | 3 | |
| | | | 15 | 4 | | | | – | – | 4 | |
| Input High Voltage, $V_{IH}$ Min. | | | 5 | 3.5 | | | | 3.5 | – | – | |
| | | | 10 | 7 | | | | 7 | – | – | |
| | | | 15 | 11 | | | | 11 | – | – | |

* Determined by minimum feasible leakage measurement for automatic testing.

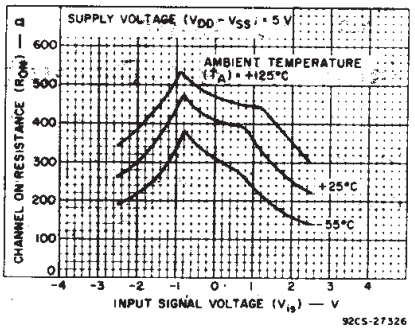



*Fig. 3—Typical ON resistance vs. input signal voltage (all types).*

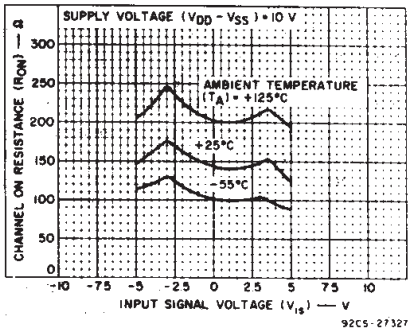



*Fig. 4—Typical ON resistance vs. input signal voltage (all types).*

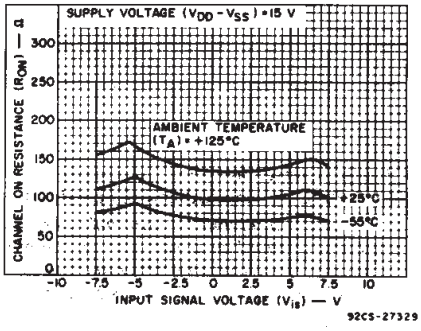



*Fig. 5—Typical ON resistance vs. input signal voltage (all types).*

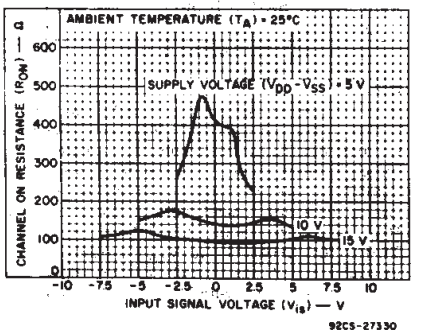


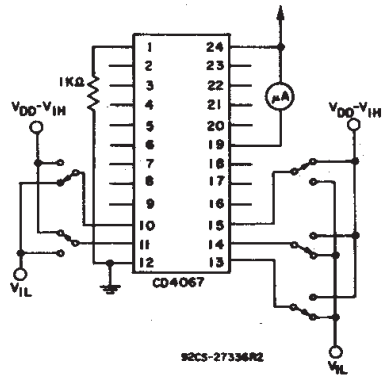

*Fig. 6—Typical ON resistance vs. input signal voltage (all types).*

## ELECTRICAL CHARACTERISTICS (Cont'd)

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{is}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | |
| Input Current, $I_{IN}$ Max. | $V_{IN}$ = 0, 18 V | | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $\pm10^{-5}$ | ±0.1 | μA |
| Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON) | $R_L$ = 10 KΩ, $C_L$ = 50 pF, $t_r$, $t_f$ = 20 ns | 0 | 5 | – | – | – | – | – | 325 | 650 | ns |
| | | 0 | 10 | – | – | – | – | – | 135 | 270 | |
| | | 0 | 15 | – | – | – | – | – | 95 | 190 | |
| Address or Inhibit-to-Signal OUT (Channel turning OFF) | $R_L$ = 300 Ω, $C_L$ = 50 pF, $t_r$, $t_f$ = 20 ns | 0 | 5 | – | – | – | – | – | 220 | 440 | ns |
| | | 0 | 10 | – | – | – | – | – | 90 | 180 | |
| | | 0 | 15 | – | – | – | – | – | 65 | 130 | |
| Input Capacitance, $C_{IN}$ | Any Address or Inhibit Input | | | – | – | – | – | – | 5 | 7.5 | pF |

## MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C



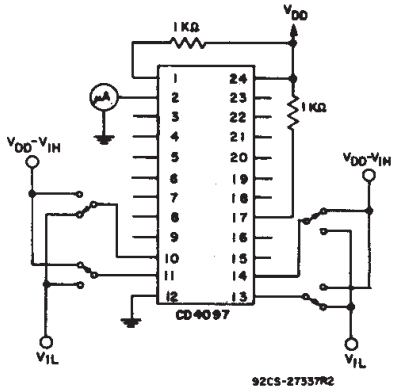




*Fig. 8—Input voltage—measure <2 μA on all OFF channels (e.g., channel 12).*

## TEST CIRCUITS

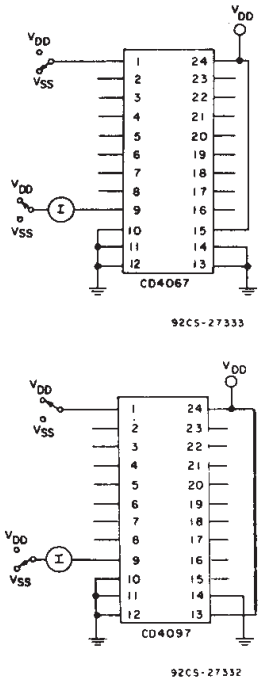



*Fig. 7—OFF channel leakage current—any channel OFF.*

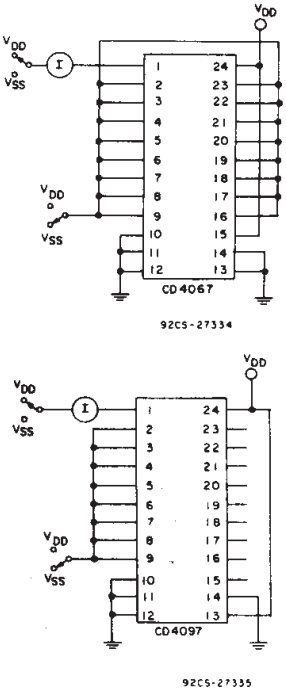



*Fig. 9—OFF channel leakage current—all channels OFF.*

## ELECTRICAL CHARACTERISTICS (Cont'd)

| CHARACTERISTIC | TEST CONDITIONS $V_{is}$ (V) | $V_{DD}$ (V) | $R_L$ (KΩ) | | | TYPICAL VALUES | UNITS |
|---|---|---|---|---|---|---|---|
| Cutoff (−3-dB) Frequency Channel ON (Sine Wave Input) | 5● | 10 | 1 | $V_{os}$ at Common OUT/IN | CD4067 | 14 | MHz |
| | $20 \log \frac{V_{os}}{V_{is}} = -3$ dB | | | | CD4097 | 20 | |
| | | | | $V_{os}$ at Any Channel | | 60 | |
| Total Harmonic Distortion, THD | 2● | 5 | 10 | | | 0.3 | % |
| | 3● | 10 | | | | 0.2 | |
| | 5● | 15 | | | | 0.12 | |
| | $f_{is}$ = 1 kHz sine wave | | | | | | |
| −40-dB Feedthrough Frequency (All Channels OFF | 5● | 10 | 1 | $V_{os}$ at Common OUT/IN | CD4067 | 20 | MHz |
| | $20 \log \frac{V_{os}}{V_{is}} = -40$ dB | | | | CD4097 | 12 | |
| | | | | $V_{os}$ at Any Channel | | 8 | |
| Signal Crosstalk (Frequency at −40 dB) | 5● | 10 | 1 | Between Any 2 Channels▲ | | 1 | MHz |
| | $20 \log \frac{V_{os}}{V_{is}} = -40$ dB | | | Between Sections CD4097 Only | Measured on Common | 10 | |
| | | | | | Measured on Any Channel | 18 | |
| Address-or-Inhibit-to-Signal Crosstalk | — | 10 | 10* | | | 75 | mV (Peak) |
| | $V_{SS}$=0, $t_r$,$t_f$=20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave) | | | | | | |

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$.

▲ Worst case.

* Both ends of channel.

## TEST CIRCUITS (Cont'd)

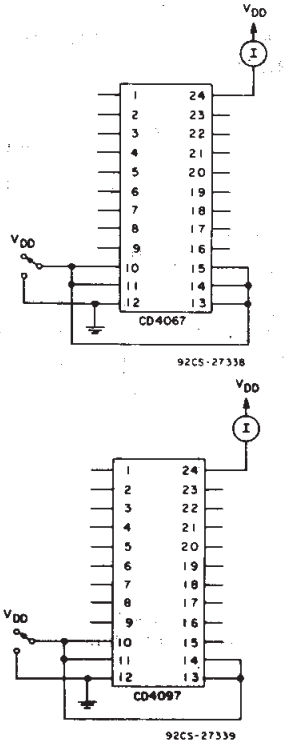
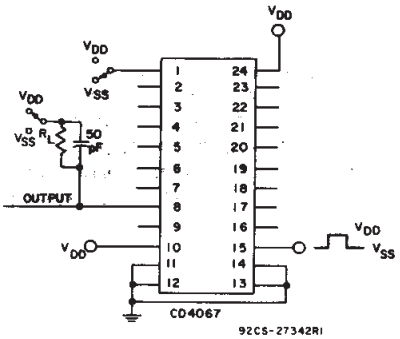



*Fig. 10— Quiescent device current.*



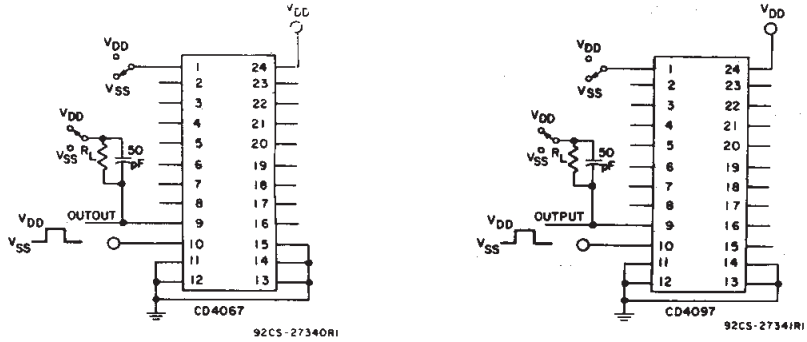




*Fig. 11— Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).*

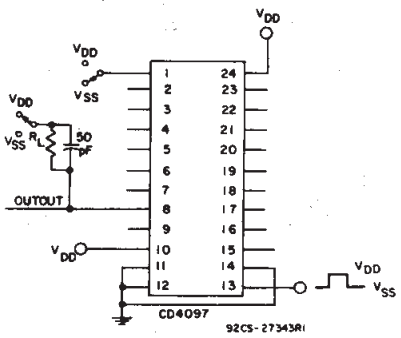



*Fig. 12— Turn-on and turn-off propagation delay—inhibit input to signal output (e.g. measured on channel 1).*

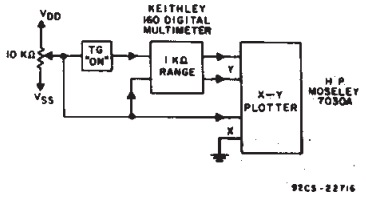



Fig. 13– Channel ON resistance measurement circuit.

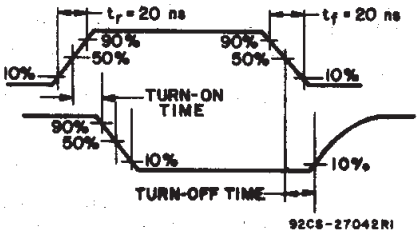



Fig. 14– Propagation delay waveform channel being turned ON ($R_L$ = 10 K Ω, $C_L$ = 50 pF).

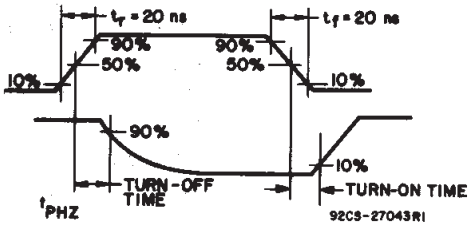



Fig. 15– Propagation delay waveform, channel being turned OFF ($R_L$ = 300 Ω, $C_L$ = 50 pF).

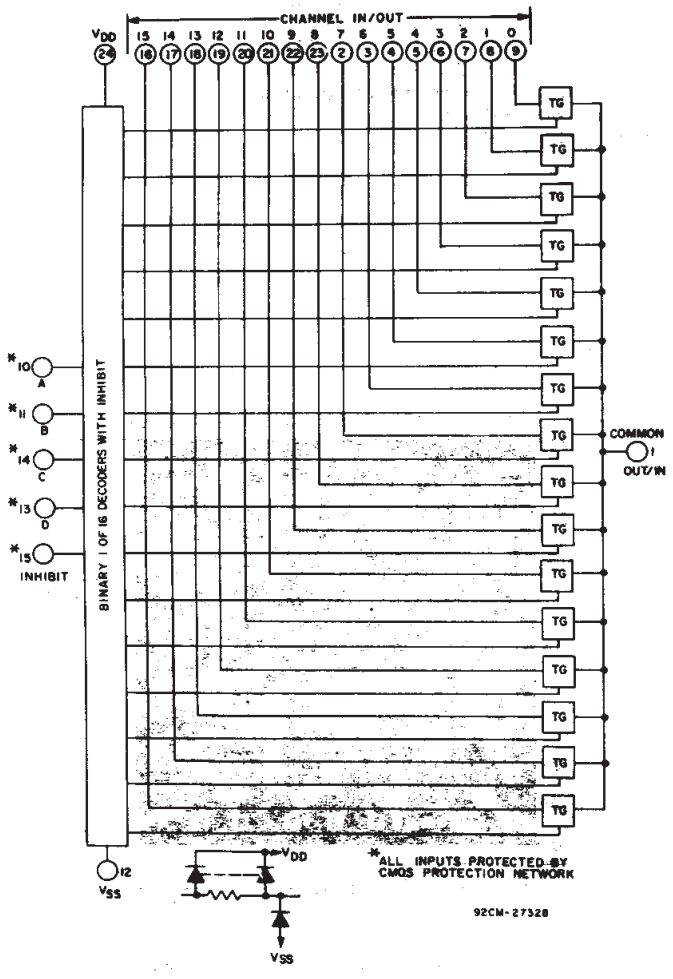



Fig. 16–CD4067 logic diagram.

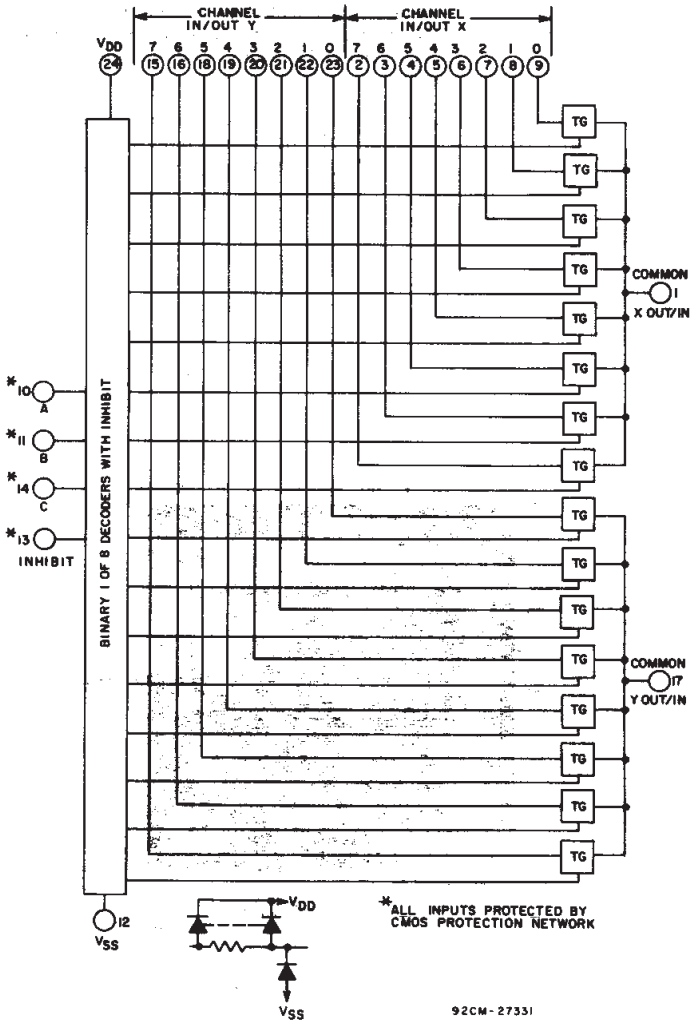



Fig. 17–CD4097 logic diagram.

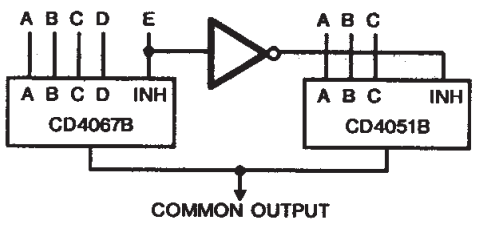



Fig. 18–24-to-1 MUX Addressing

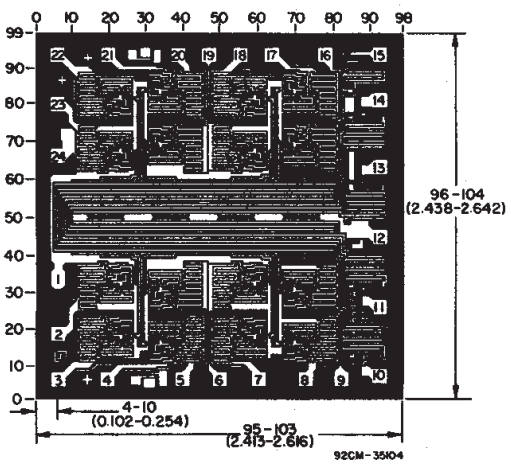
## SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive $V_{DD}$ and the signal inputs, the $V_{DD}$ current capability should exceed $V_{DD}/R_L$ ($R_L$=effective external load). This provision avoids permanent current flow or clamp action on the $V_{DD}$ supply when power is applied or removed from the CD4067B or CD4097B.

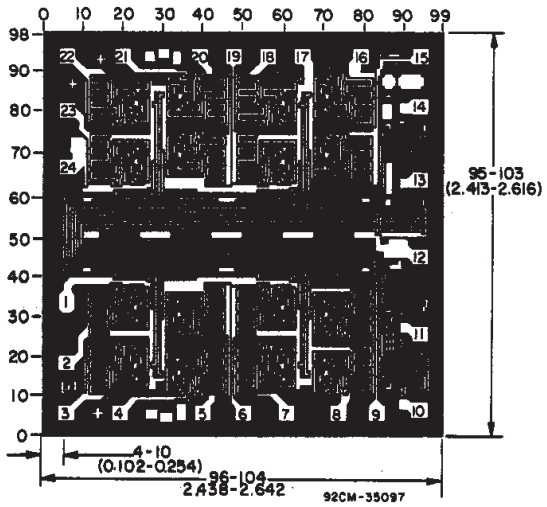
When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to $V_{SS}$, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to $V_{SS}$.

The amount of charge dumped is mostly a function of the signal level above $V_{SS}$. Typically, at $V_{DD}-V_{SS}$=10 V, a 100-pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to $V_{SS}$. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from $R_{ON}$ values shown in ELECTRICAL CHARACTERISTICS CHART). No $V_{DD}$ current will flow through $R_L$ if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.




*Dimensions and pad layout for CD4067BH.*




*Dimensions and pad layout for CD4097BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4067BE | LIFEBUY | PDIP | N | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4067BE | |
| CD4067BEE4 | LIFEBUY | PDIP | N | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4067BE | |
| CD4067BF | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | CD4067BF | Samples |
| CD4067BF3A | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | CD4067BF3A | Samples |
| CD4067BM | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4067BM | Samples |
| CD4067BM96 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -55 to 125 | CD4067BM | Samples |
| CD4067BM96E4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4067BM | Samples |
| CD4067BM96G4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4067BM | Samples |
| CD4067BME4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4067BM | Samples |
| CD4067BPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM067B | Samples |
| CD4067BPWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM067B | Samples |
| CD4067BPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM067B | Samples |
| CD4097BE | LIFEBUY | PDIP | N | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4097BE | |
| CD4097BF | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | CD4097BF | Samples |
| CD4097BM | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4097BM | Samples |
| CD4097BME4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4097BM | Samples |
| CD4097BMG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4097BM | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4097BPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM097B | Samples |
| CD4097BPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM097B | Samples |
| CD4097BPWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM097B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4067B, CD4067B-MIL, CD4097B, CD4097B-MIL :**

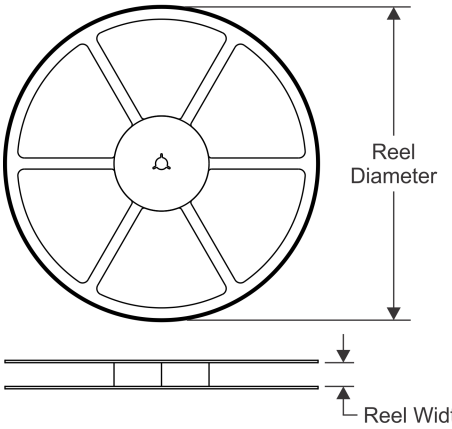
- Catalog: CD4067B, CD4097B
- Military: CD4067B-MIL, CD4097B-MIL

NOTE: Qualified Version Definitions:

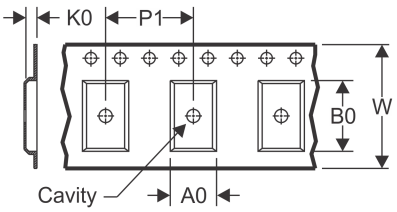
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

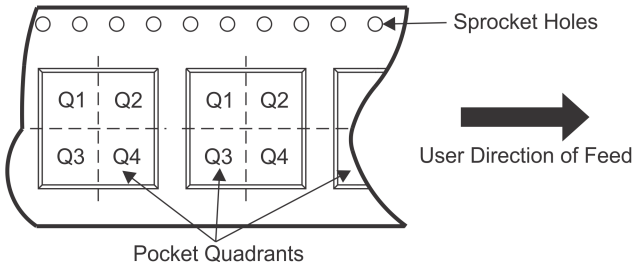



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

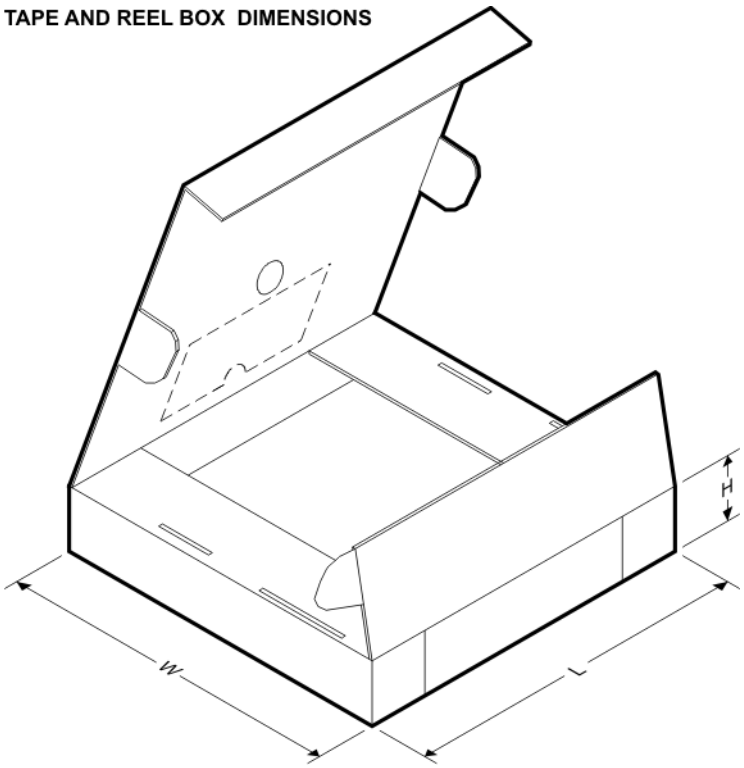
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4067BM96 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CD4067BM96 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CD4067BM96G4 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CD4067BPWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| CD4097BPWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

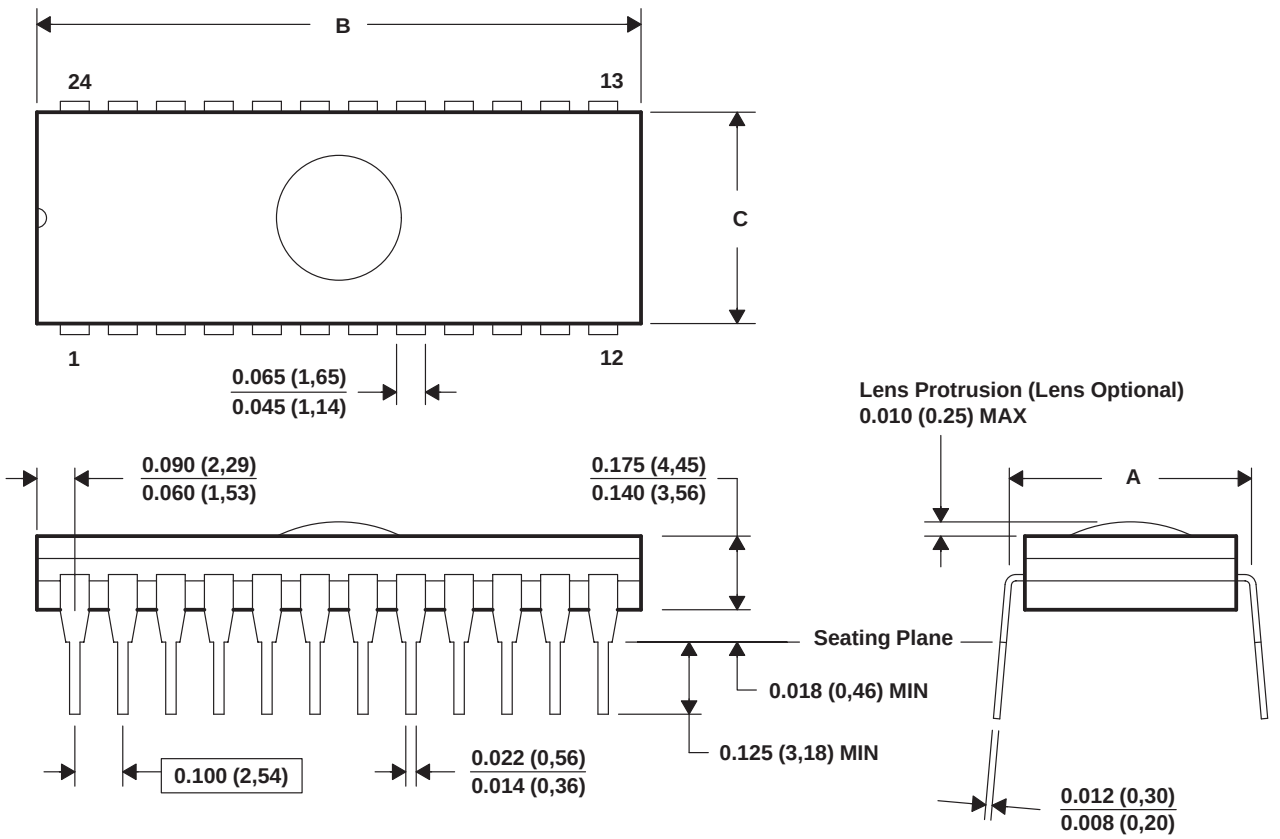
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD4067BM96 | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| CD4067BM96 | SOIC | DW | 24 | 2000 | 364.0 | 361.0 | 36.0 |
| CD4067BM96G4 | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| CD4067BPWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4097BPWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |

MCDI004A – JANUARY 1995 – REVISED NOVEMBER 1997

## J (R-GDIP-T**)

## CERAMIC DUAL-IN-LINE PACKAGE

**24 PINS SHOWN**




| DIM \ PINS ** | | 24 | | 28 | | 32 | | 40 | |
|---|---|---|---|---|---|---|---|---|---|
| | | NARR | WIDE | NARR | WIDE | NARR | WIDE | NARR | WIDE |
| "A" | MAX | 0.624(15,85) | 0.624(15,85) | 0.624(15,85) | 0.624(15,85) | 0.624(15,85) | 0.624(15,85) | 0.624(15,85) | 0.624(15,85) |
| | MIN | 0.590(14,99) | 0.590(14,99) | 0.590(14,99) | 0.590(14,99) | 0.590(14,99) | 0.590(14,99) | 0.590(14,99) | 0.590(14,99) |
| "B" | MAX | 1.265(32,13) | 1.265(32,13) | 1.465(37,21) | 1.465(37,21) | 1.668(42,37) | 1.668(42,37) | 2.068(52,53) | 2.068(52,53) |
| | MIN | 1.235(31,37) | 1.235(31,37) | 1.435(36,45) | 1.435(36,45) | 1.632(41,45) | 1.632(41,45) | 2.032(51,61) | 2.032(51,61) |
| "C" | MAX | 0.541(13,74) | 0.598(15,19) | 0.541(13,74) | 0.598(15,19) | 0.541(13,74) | 0.598(15,19) | 0.541(13,74) | 0.598(15,19) |
| | MIN | 0.514(13,06) | 0.571(14,50) | 0.514(13,06) | 0.571(14,50) | 0.514(13,06) | 0.571(14,50) | 0.514(13,06) | 0.571(14,50) |

**4040084/C 10/97**

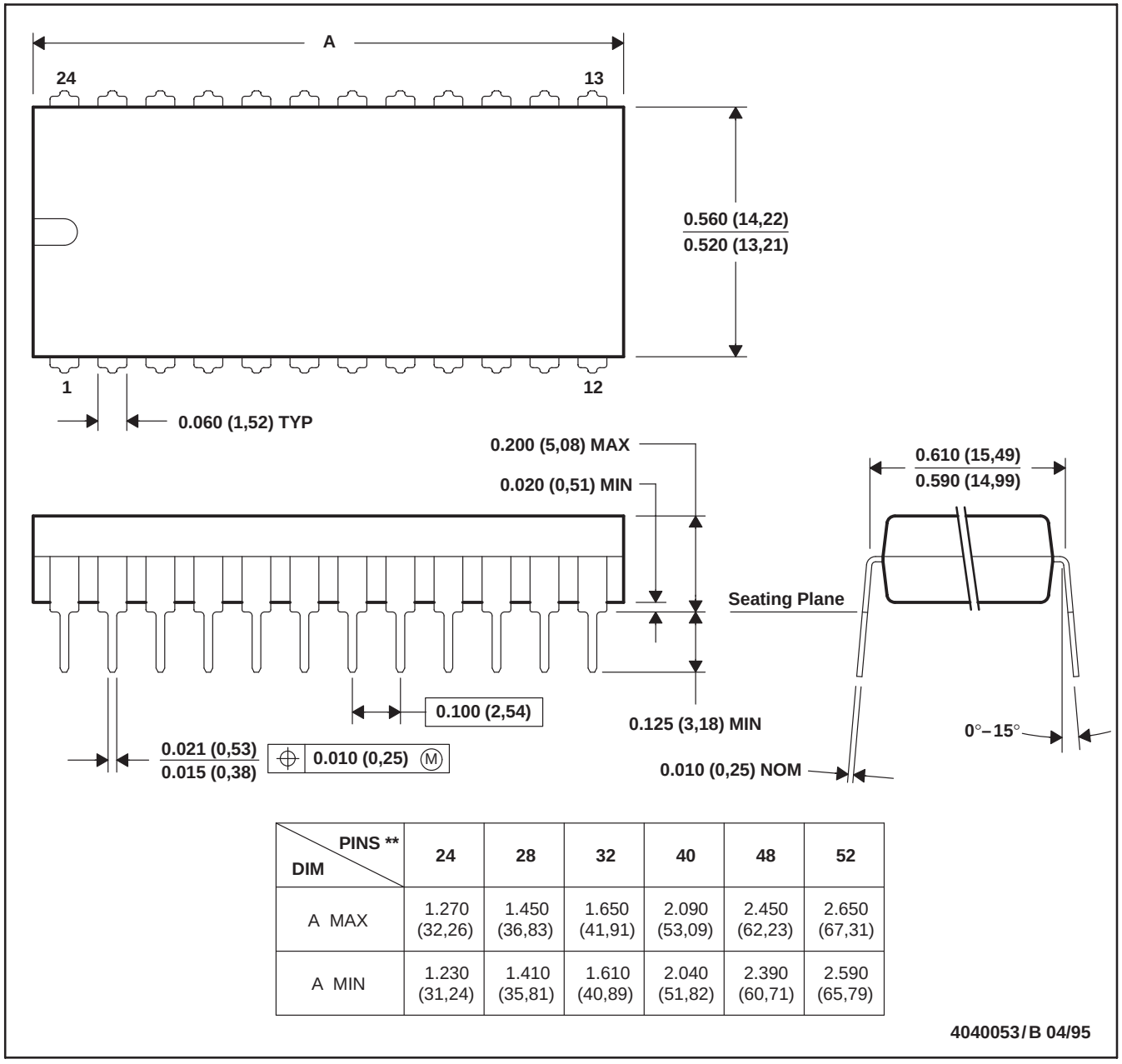
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

MPDI008 – OCTOBER 1994

## N (R-PDIP-T**)

## PLASTIC DUAL-IN-LINE PACKAGE

**24 PIN SHOWN**

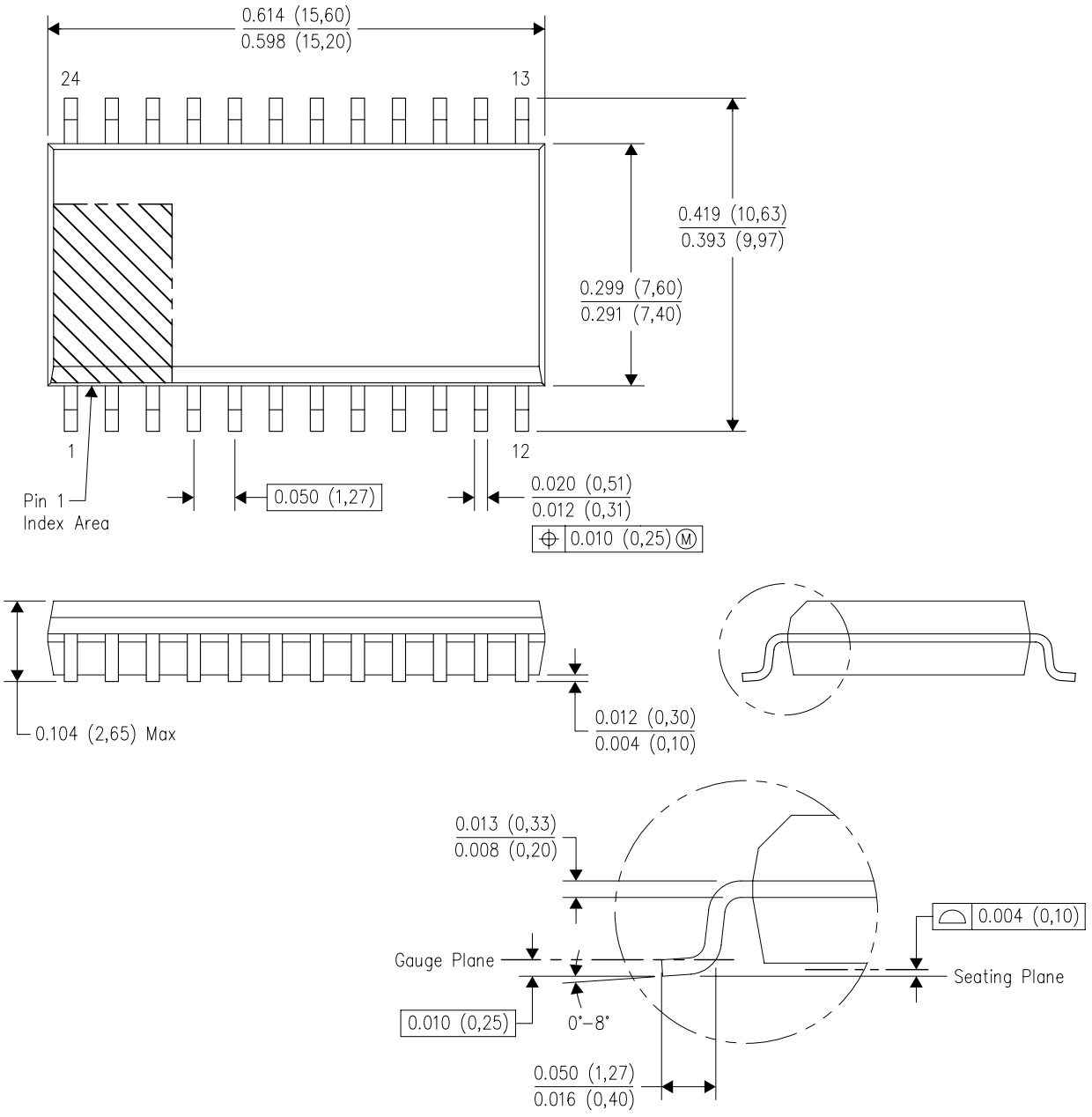



| DIM \ PINS ** | 24 | 28 | 32 | 40 | 48 | 52 |
|---|---|---|---|---|---|---|
| A MAX | 1.270 (32,26) | 1.450 (36,83) | 1.650 (41,91) | 2.090 (53,09) | 2.450 (62,23) | 2.650 (67,31) |
| A MIN | 1.230 (31,24) | 1.410 (35,81) | 1.610 (40,89) | 2.040 (51,82) | 2.390 (60,71) | 2.590 (65,79) |

**4040053/B 04/95**

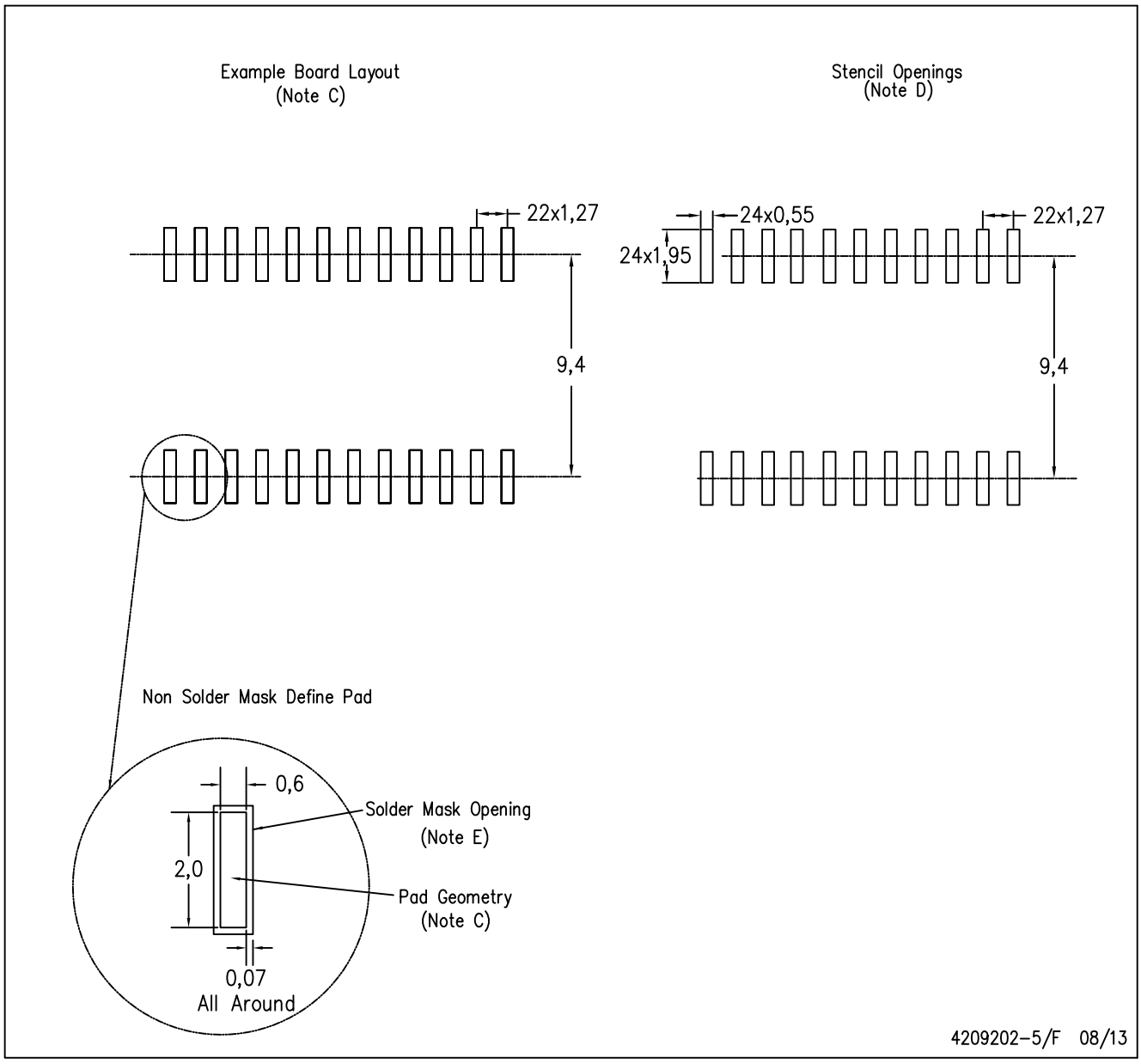
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



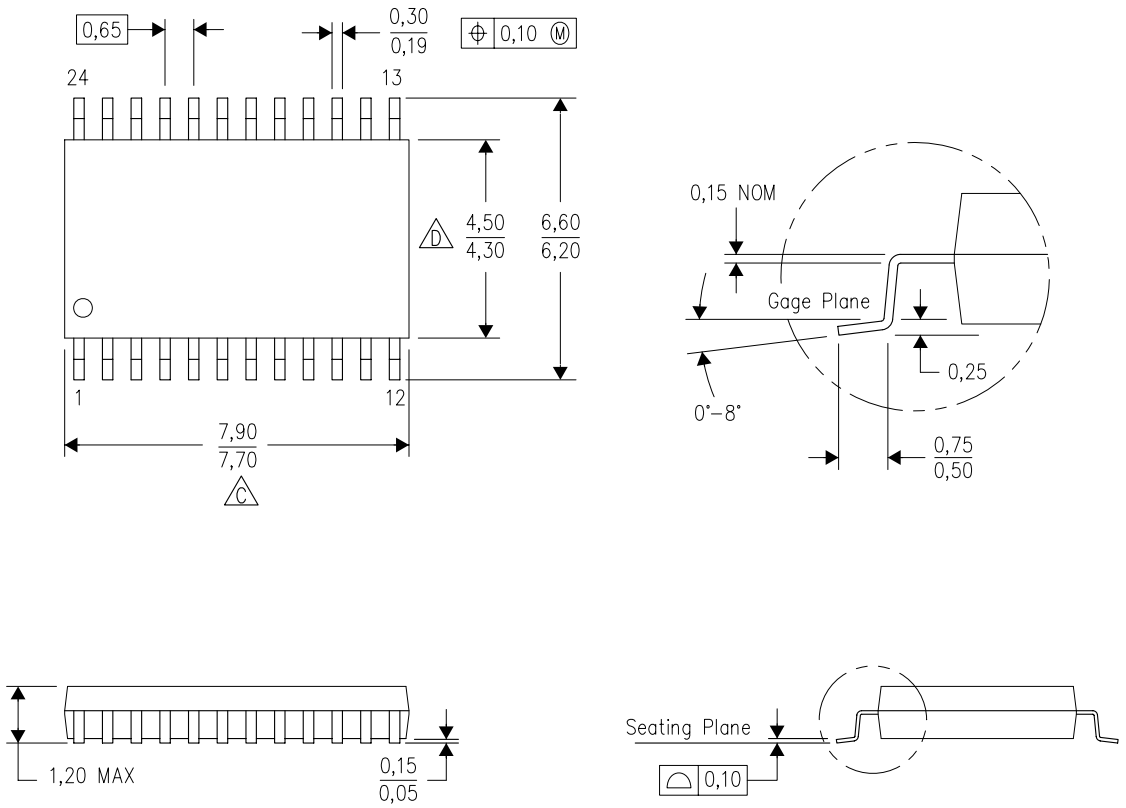

NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

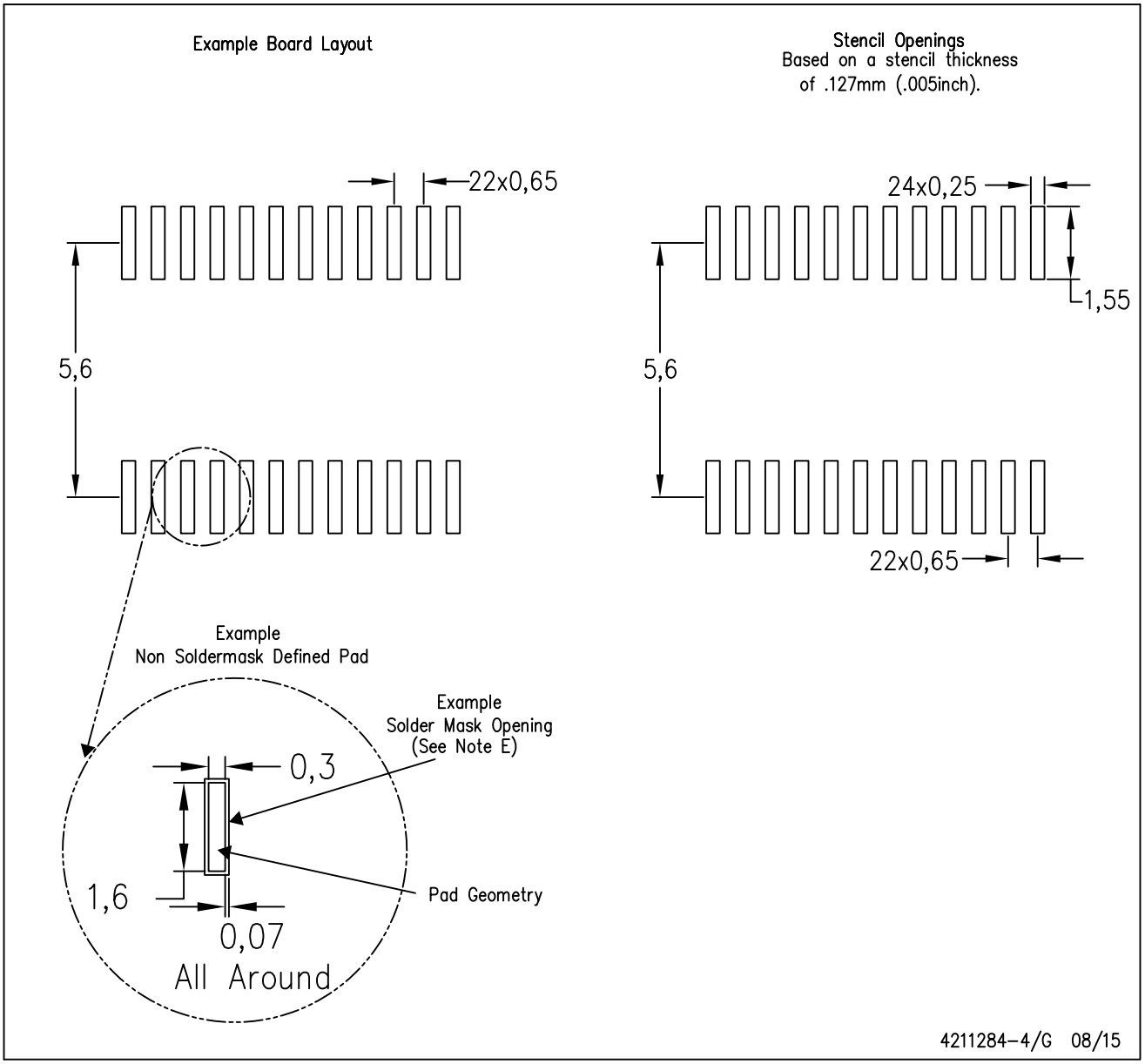
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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